(C) AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor MOSFET structure having improved electrostatic discharge tolerance, the structure comprising:

a semiconductor substrate having an active device surface;

in said surface, a MOSFET source region and a MOSFET drain region separated by a channel region;

a P-type dopant region subjacent said drain region and having a dopant concentration and predetermined dimensions [[~~such~~]] selected for increasing inherent parasitic transistor gain of said MOSFET structure [[~~is increased~~]] for improving said electrostatic discharge tolerance.

2. (Original) The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set for increasing drain-to-substrate capacitance thereby.

3. (Original) The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set such that the MOSFET trigger voltage is decreased thereby.

4. (Original) The structure as set forth claim 1 wherein breakdown voltage of said parasitic transistor is tailored by depth of the P-type dopant region with respect to said surface and said substrate.

5. (Currently Amended) The structure as set forth in claim 1 wherein said MOSFET is a N-channel MOSFET located in a P-type dopant well in said epitaxial layer and surface concentration of the dopant ions in the P-deep region is approximately an order

of magnitude greater than that of the dopant ions at the P-well [[~~209~~]] surface concentration.

6. (Currently Amended) The structure as set forth in claim 3 comprising:

a pair of MOSFETs, including a paired N-MOSFET, and a paired P-MOSFET, wherein said paired N-MOSFET and said paired P-MOSFET are connected in a push-pull configuration.

7. (Original) The structure as set forth in claim 6 wherein the P-deep implant region in both the P-MOSFET and the N-MOSFET reduces effective base width of parasitic transistors therein via reduction of substrate-to-drain spacing.